REMARKS

Claim 20 has been canceled without prejudice, and claims 18, 21-23, and 26-28 have been amended. Therefore, claims 18, 19 and 21-35 are currently pending. No new matter has been added. Reconsideration of the present application is requested.

As an initial matter, Applicants gratefully acknowledge the indication by the Examiner that claims 23, 26 and 28 contain allowable subject matter. Claims 23, 26 and 28 have been rewritten in independent form. It is submitted that claims 23, 26 and 28 are now in condition for allowance.

The Examiner has indicated that Applicants have not submitted a certified ***translation*** of Applicants' German priority application. Respectfully, Applicants believe that a translation is not required, but rather that a certified ***copy*** of the German priority application is required. Applicants are in the process of obtaining a certified copy of the German priority application, and will submit it as soon as it is received.

Claims 18-22, 24, 25, 27, 29 and 35 have been rejected under 35 U.S.C. §102(b) as anticipated by Hefner (U.S. Patent No. 4,566,102). It is respectfully submitted that Hefner does not anticipate any of claims 18-22, 24, 25, 27, 29 and 35, for at least the following reasons.

Claim 18 recites, *inter alia*, a control that controls the at least one input multiplexer and the at least one output multiplexer, the control using a single decoder.

Hefner purports to disclose a chip array configuration in which an A/B CTL line gates (DOT-ORs) chip inputs to separate buses A and B, and in which output buses are also "DOT-OR'ed" between adjacent chips such that when a particular bus A/B is not selected, zeroes appear on the outputs. Hefner, col. 3, lines 19-30. It is understood that the setting of the bytes on the A/B CTL line occurs through use of a first decoder. In addition, Hefner provides for CIPT (Chip-In-Place-Test) inputs that are used to degate both outputs of a given chip. Hefner, col. 3, lines 30-35. In this regard, Hefner calls for two separate codes to be used to reconfigure the chip array in order to exclude a defective chip, i.e., a code on the A/B CTL line to drive the A and B buses to avoid inputs to the defective chip, and a code on the CIPT outputs to degate the defective chip outputs. See Hefner, col. 4, lines 4-23.

In contrast, according to claim 18, input and output multiplexers are used to switch input and output signals to the modules, respectively, instead of DOT-OR

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circuits. Furthermore, the input and output multiplexers are controlled using a single decoder. For example, as shown in Figure 1, a single decoder (0107) which receives data concerning the location of a defective module operatively switches both the input and the output multiplexers to exclude the defective module.

The features of claim 18 provide certain advantages that the arrangements of the Hefner reference do not provide -- and are not intended to provide -- since they are designed to operate at the chip level rather than within an integrated circuit. Because the present invention refers to the replacement of busses and functional units within a single integrated circuit, it avoids the added complexity of two control buses and decoders by implementing a single decoder that provides the select signal for both groups of multiplexers. This not only reduces the power consumption of the overall circuitry but also allows for easier testing.

For the reasons given above, it is respectfully submitted that Hefner does not disclose all of the features of independent claim 18, or of claims 19, 21, 22, 24, and 25 which depend from claim 18.

As regards independent claim 27, it recites, as amended, a method for testing an integrated circuit having cells including, inter alia, testing a cell function of the integrated circuit by executing, with the cells, a test program including calculating test vectors, and performing, with at least one of the cells wired as a comparator, a comparison between a test result and a setpoint result. The specification of the present invention provides support for these features at e.g., page 6, lines 31-35, which states that the modules (PAEs) are "wired as comparators so that the values calculated on the basis of the test vectors are compared to the setpoint results."

Hefner refers to latching array outputs to an output register where parity checking is done to detect array failures. This arrangement differs from Applicants recited arrangement in which failures are detected by wiring the modules as comparators. For at least this reason, it is submitted that Hefner does not disclose all of the features of claim 27.

It is additionally noted with respect to claim 29 that Hefner uses a separate maintenance processor for testing operations and therefore does not call up test data from an integrated memory in the integrated circuit during, for example, booting or resetting, so that the data can be immediately used without separate processing. Therefore, for this additional reason, it is submitted that Hefner does not disclose all of

the features of claim 29.

In view of the foregoing, withdrawal of the rejection of claims 18, 19, 21, 22, 24, 25, 27 and 29 under 35 U.S.C. §102(b) based on the Hefner reference is respectfully requested.

Claims 31 and 33 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hefner in view of Matsumoto (U.S. Patent No. 5,657,330). It is respectfully submitted that neither claim 31 nor claim 33 is obvious over Matsumoto, for at least the following reasons.

Claims 31 and 33 depend from claim 27. As Matsumoto does not cure the deficiencies of the Hefner reference discussed above with respect to claim 27, in that it also does not disclose or render obvious performing, with at least one of the cells wired as a comparator, a comparison between a test result and a setpoint result, it is respectfully submitted that claims 31 and 33 are not rendered obvious by the combination of Hefner and Matsumoto.

Claim 34 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Hefner in view of Matsumoto and further in view of Takano (U.S. Patent No. 5,530,873). It is respectfully submitted that claim 34 is not obvious over Hefner in view of Matsumoto and Takano, for at least the following reasons.

Claim 34 depends from claim 27. As Takano fails to cure the deficiencies of Hefner and Matsumoto with respect to the features of claim 27 in that it also does not render obvious performing, with at least one of the cells wired as a comparator, a comparison between a test result and a setpoint result, it is respectfully submitted that claim 34 is not rendered obvious by the combination of Hefner, Matsumoto and Takano.

Claims 30 and 32 have has been rejected under 35 U.S.C. §103(a) as being unpatentable over Hefner in view of Bouvier et al. (U.S. Patent No. 5,530,946). It is respectfully submitted that Hefner in view of Bouvier does not render obvious claims 30 and 32, for at least the following reasons.

Claims 30 and 32 depend from claim 27. Bouvier similarly does not cure the deficiencies of the Hefner reference and does not render obvious the features of claim 27. Therefore, claims 30 and 32 are not rendered obvious by the combination of Hefner and Bouvier.

In view of the foregoing, withdrawal of the obviousness rejections is

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respectfully requested.

CONCLUSION

All issues having been addressed, it is believed that the present application is in condition for allowance. Prompt reconsideration and allowance of the present application are respectfully requested.

Respectfully submitted,

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